EXPERIMENT 1



AND Gates & OR Gates

OBJECTIVES:

This experiment shows the students how to:

- Create new projects and save schematic designs in Xilinx ISE Software(CPLD-Complex Programmable logic device)
- Download JEDHC files to the target board.
- Demonstrate the characteristics of AND and OR gates.
- Develop truth tables for AND and OR gates.

MATERIALS:

- Xilinx Vivado software, student or professional edition V2018.2 or higher.
- IBM or compatible computer with Pentium III or higher, 128 M-byte RAM or more, and 8 G-byte Or larger hard drive.
- BASYS 3 Board.

DISCUSSION:

AND and OR gates are hardware implementations of the two fundamental Boolean operations: logical multiplication (AND) and logical addition (OR). They are represented on a diagram by gate symbols, and their characteristics can be described by truth tables, Boolean equations, and timing waveforms. Both AND and OR gates can have two or more inputs, but only one output. Although we use two inputs in our discussion, the principles apply to more than two inputs.

Gate Characteristics:

1. The AND Gate

Symbol	Boolean Equation		Truth T	able
		Inp	outs	Output
Δ		Α	B	X
[™] ⊒_)- x	X=AB	0	0	0
		0	1	0
		1	0	0
		1	1	1
		<u></u>		

The behavior of an AND gate can be summarized as follows: The output is HIGH (true or logic'1') only when all the inputs are HIGH. If any of the inputs is LOW (false or logic 0), the output will be LOW.

Page 2 | 18

2. The OR Gate

Symbol	Boolean Equation		Truth Ta	able
		Inj	puts	Output
		Α	В	X
A	Y = A + B	0	0	0
$B \rightarrow Y$	1 11 D	0	1	1
en e		1	0	1
		1	1	1
		<u>[</u>	1	J

As seen from the above truth table, the output is LOW only when all the inputs are LOW. If any of the inputs is HIGH, then the output is HIGH.

For both AND gates and OR gates, the output goes HIGH when the required HIGH logic levels are applied to the input. We describe this by saying that AND gates and OR gates have active-high inputs and active-high outputs.

PROCEDURE:

1. Open Xilinix Vivado.

2. In the Xilinx-Project Navigator window, Quick start, New Project.

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HLLX Editions	Create a New Vivado Project This wizard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.	
E XILINX.	< <u>B</u> ack <u>Next></u> Einish Cance l	

3. Name the project.

Page 4 | 18

🝌 New Project	
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Project name:	project
New Project	holec
Project Type Specify the type of	f project to create.
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Do not	t specify sources at this time
Post-synt implemen	hesis Project: You will be able to add sources, view device resources, run design analysis, planning ar ntation. I soecify sources at this time
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5. Select New Source... and the New window appears. In the New window, choose Schematic, type your file name (such as *source_1*) in the File Name editor box, click on OK, and then click on the Next button.

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7. The Define Module Window that will appear, we will choose the input and output labels for the gates under investigation in this experiment. In this experiment, we are investigating a 3-input AND gate and 3-input OR. Then Under "Port Name", add "A0", "A1", "A2" as inputs for AND gate, add "B0", "B1", "B2" as inputs for OR gate. Then add "X" & "Y" as outputs for the mentioned gates and select OK.

a module a each port spe B and LSB v orts with blank	and sp cified: alues v c name	ecify I/ will be s will i	o Ports ignore not be	to add t d unless written.	its Bus	source file. s column is checked.
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A1	in	~		0	0	
A2	in	~		0	0	
B0	in	~		0	0	
B1	in	~		0	0	
B2	in	~		0	0	
х	out	~		0	0	
Y	out	~		0	0	

8. In the "source_1.vhd" created file, type the gates equivalent VHDL code for the AND & OR gates between the "begin" and "end Behavioral" as follows and then save the file.





9. Next, we need to add To add a constraint file with the".xdc" extension, as following: Go to "Flow Navigator" and from "Project Manager" select "Add Sources" then "Add or create constraints". Next, choose "Create File" and enter the file name "lab_2" then "OK" followed by "Finish".

Specify constraint set	1 (a) Create Constraints File X Create a new constraints file and add it to your project Image: Create file Elie type: XDC Image: Create file File location: Image: Create file Image: Create file Add Files Create File Image: Create file
3	<back next=""> Einish Cancel</back>

10. Then, we need to get a template xdc file that is going to be edited according to the different experiments. Google "basys 3 xdc file" and choose the "xilinix" link that appears (<u>https://www.xilinx.com/support/documentation/university/Vivado-Teaching/HDL-Design/2015x/Basys3/Supporting%20Material/Basys3_Master.xdc</u>).

Page 10 | 18

Copy the whole file and paste it into the "lab_2.xdc" that you have just created in the last step. Then uncomment and edit the input Switches and the output LEDs as in the next step.

11. Uncomment (by deleting the # sign) sw[0], sw[1], sw[3],.... led[0], led[1],...
lines. Note that each of them has two successive lines (Uncomment both of them). Do the following replacements: sw[0] → A0, sw[1] → A1,...., led[0] → X, led[1] → Y,..., then Save the file

12. From the tool tab choose the play button and then "Run Implementation". Select "Number of jobs" =1 and then press OK.

À Launch Runs		×
Launch the selected	synthesis or implementation runs.	A
Launch <u>d</u> irectory:	■ <default directory="" launch=""></default>	~
Options		
● <u>L</u> aunch run ○ <u>G</u> enerate s	s on local host: Number of jobs: 1	~
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	ок	Cancel
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13. The implementation errors window will appear if any or the successfully completed window. From this window select "Generate Bitstream" and then OK. This will make the software generate ".bin" file to be used in programing the hardware BAYAS 3.

Implementation Completed				
Implementation succes	ssfully completed.			
O Open Implemented De	esign			
Generate Bitstream				
○ <u>V</u> iew Reports				
Don't show this dialog aga	ain			
ок	Cancel			

14. The next window will appear in which choose "Open Hardware Manger", connect the Hardware Kit to the USB port and then press OK.



15. A green tab will appear in the top of the Vivado window, from which choose "open target" to program the hardware.

HARDWARE MANAGER - unconnected		? ×
No hardware target is open. Open target		
Hardware ? _ D 🖾 ×	source_1.whd x lab_2.xdc x	? 🗆 🖸
$ Q_{n} \underset{\sim}{\times} \Leftrightarrow \not g \models \gg \blacksquare \qquad \Leftrightarrow$	C/XillinxI/Ivadoi2018.2lproject.project.srcs/sources_1/hew/source_1.vhd	×
No content	Q	☆
Source File Properties ? _ D 🖸 X	39 B1 : in STD_LOGIC; 40 B2 : in STD_LOGIC;	
● source_1.vhd ← → ✿	41 C : In STU_LUBLIC; 42 X : out STD_LUGIC;	
C Enabled Location: C/Xilm/Wvado/2018.2/project/project. Type: VHDL Library: ai_defaultib Stze: 1.3 KB Modified: Today at 16.27.53 PM	<pre>43 Y : out STD_LOGIC; 44 2 : out STD_LOGIC; 45 G end source_l: 47 architecture Behavioral of source_l is 48 beet 50 X <= (AO HAND A1) HAND A2;3 input NAND Gate 51 X <= (AO HAND A1) HAND A2;3 input NAND Gate 52 Z <= HOT C; NOT Gate 53 C 54 G end Behavioral; 55 C</pre>	

16. From the window appears, select the ".bin" file from the Project you create by browsing for the generated ".bit file" under the ".runs" folder and program the board then press OK.

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17. Notice that the 7-segment on the hardware is counting up from 0 to 9 frequently until you download the program and it will stop.



18. Fill in the following truth tables for all the gates by observing the inputs/outputs on the programmed board.

A. AND Gate

Truth Table (1)

A0	A1	A2	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Symbol

Boolean Equation

Page 15 | 18

B. OR Gate

Truth Table (2)

BO	B1	B2	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Symbol

Boolean Equation

19. Verify that the experimental results are consistent with the Discussion.

Checked by_____ Date _____

Page 16 | 18

Questions:

1.) How many rows must a truth table have in order to describe a 4-input AND gate? Which input will make the output HIGH?

2.) Which output is the unique one in a 3-input OR gate? Does it agree with the statement in our Discussion section?

3.) Sketch the output waveform for the given NEXT



4.) In the Xilinx software symbol library, the maximum number of inputs for AND and OR gales is 9. What would you do if 10-input AND and OR gales are needed? Draw the schematic diagrams and show the connections.

Page 18 | 18