EXPERIMENT 1

AND Gates & OR Gates

OBJECTIVES:

This experiment shows the students how to:

- Create new projects and save schematic designs in Xilinx ISE Software(CPLD-Complex Programmable logic device)
- Download JEDHC files to the target board.
- Demonstrate the characteristics of AND and OR gates.
- Develop truth tables for AND and OR gates.

MATERIALS:

- Xilinx Vivado software, student or professional edition V2018.2 or higher.
- IBM or compatible computer with Pentium III or higher, 128 M-byte RAM or more, and 8 G-byte Or larger hard drive.
- BASYS 3 Board.

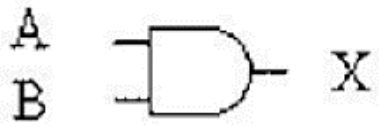
DISCUSSION:

AND and OR gates are hardware implementations of the two fundamental Boolean operations: logical multiplication (AND) and logical addition (OR). They are represented on a diagram by gate symbols, and their characteristics can be described by truth tables, Boolean equations, and timing waveforms. Both AND and OR gates can have two or more inputs, but only one output. Although we use two inputs in our discussion, the principles apply to more than two inputs.

Gate Characteristics:

1. The AND Gate

Symbol	Boolean Equation	Truth Table



X=AB

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

The behavior of an AND gate can be summarized as follows: The output is HIGH (true or logic‘1’) only when all the inputs are HIGH. If any of the inputs is LOW (false or logic 0), the output will be LOW.

2. The OR Gate

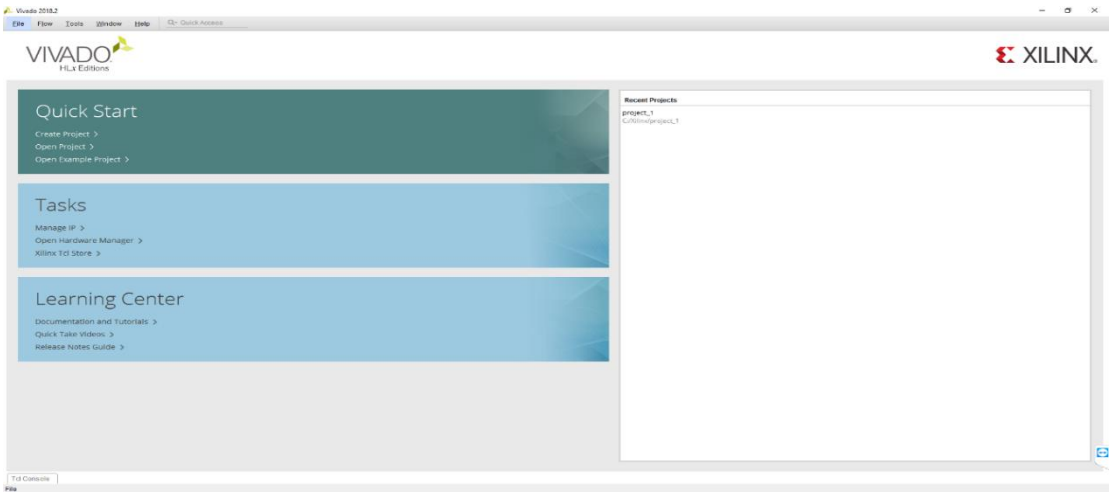
Symbol	Boolean Equation	Truth Table
	$Y=A+B$	

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

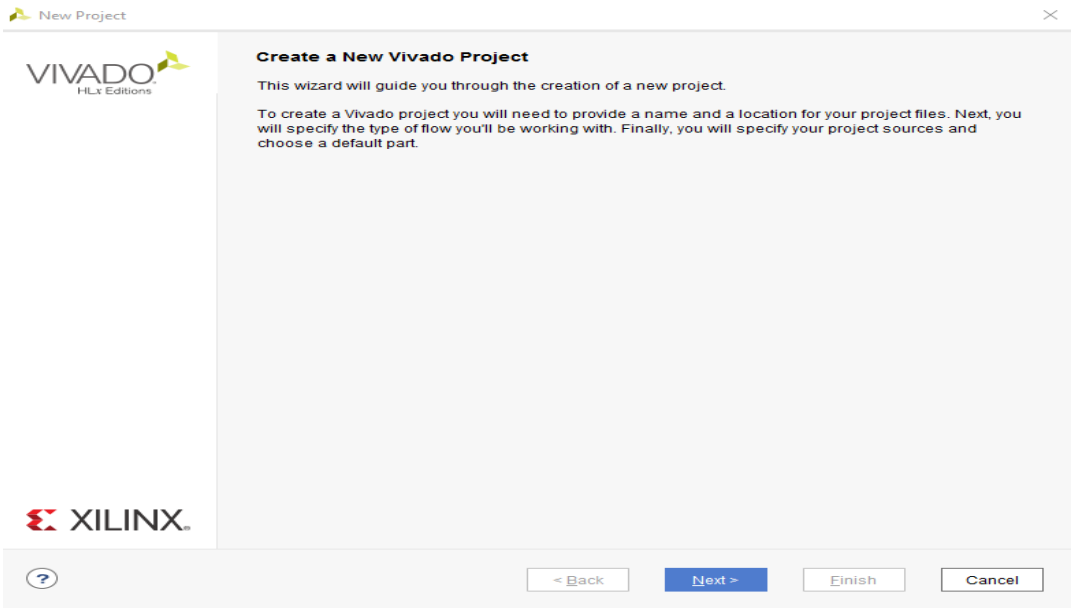
As seen from the above truth table, the output is LOW only when all the inputs are LOW. If any of the inputs is HIGH, then the output is HIGH.
For both AND gates and OR gates, the output goes HIGH when the required HIGH logic levels are applied to the input. We describe this by saying that AND gates and OR gates have active-high inputs and active-high outputs.

PROCEDURE:

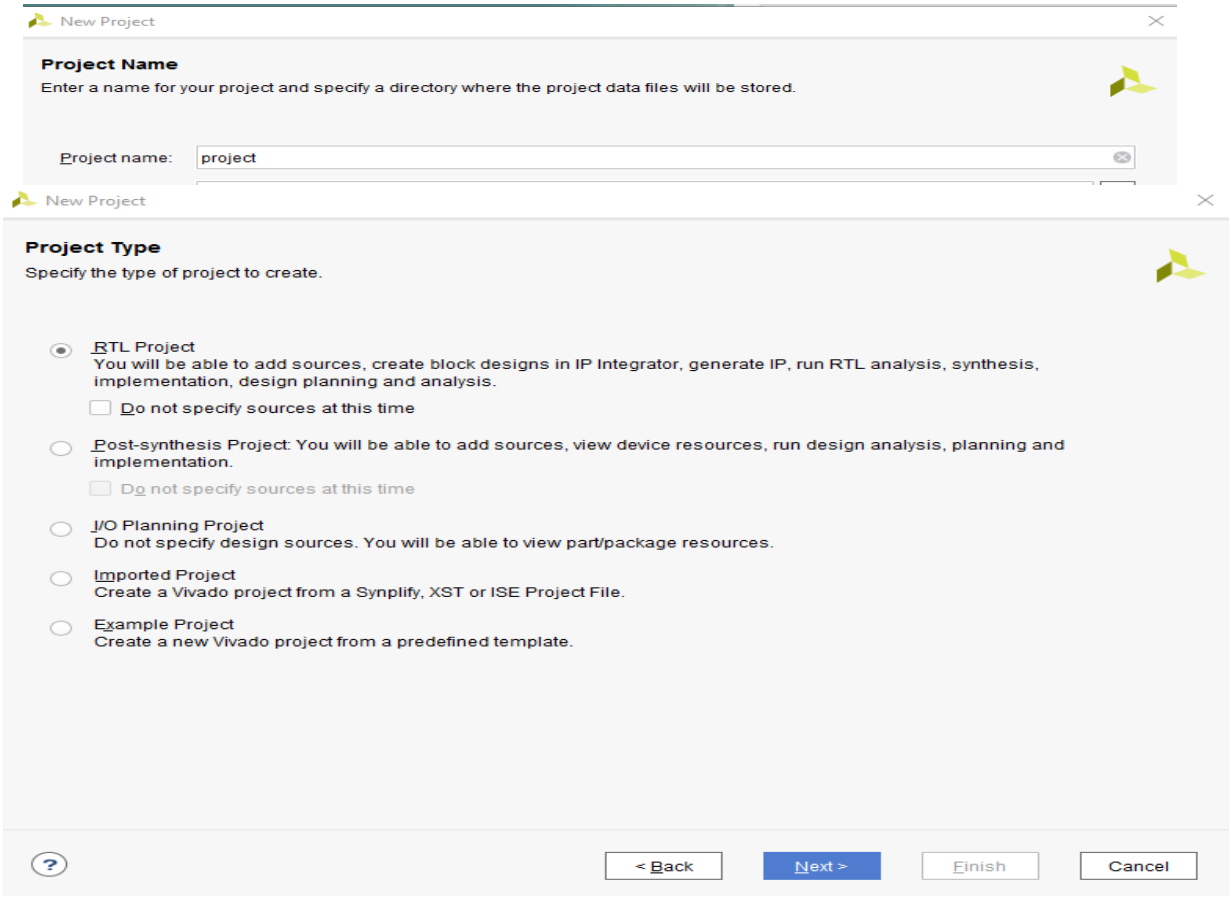
1. Open Xilinix Vivado.



2. In the **Xilinx-Project Navigator** window, Quick start, **New Project**.

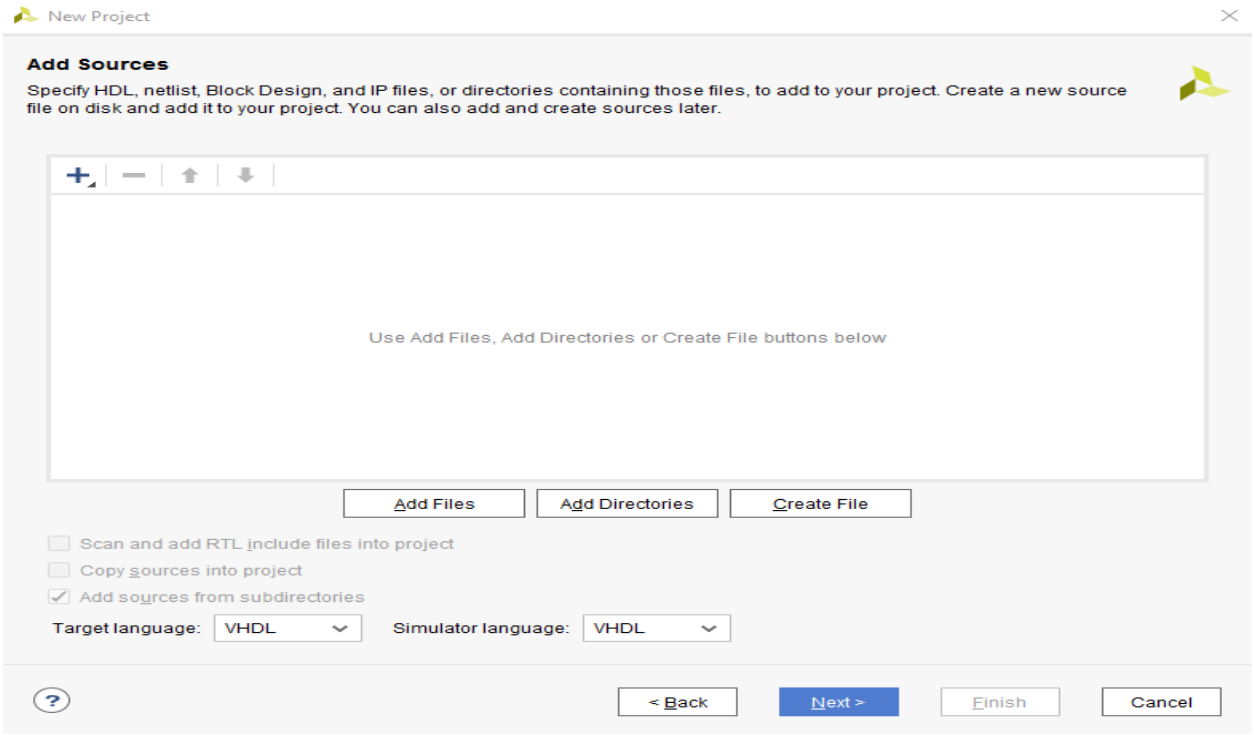


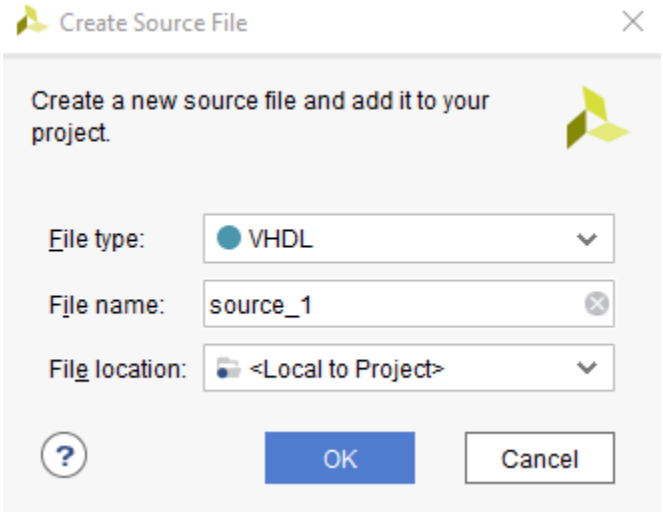
3. Name the project.

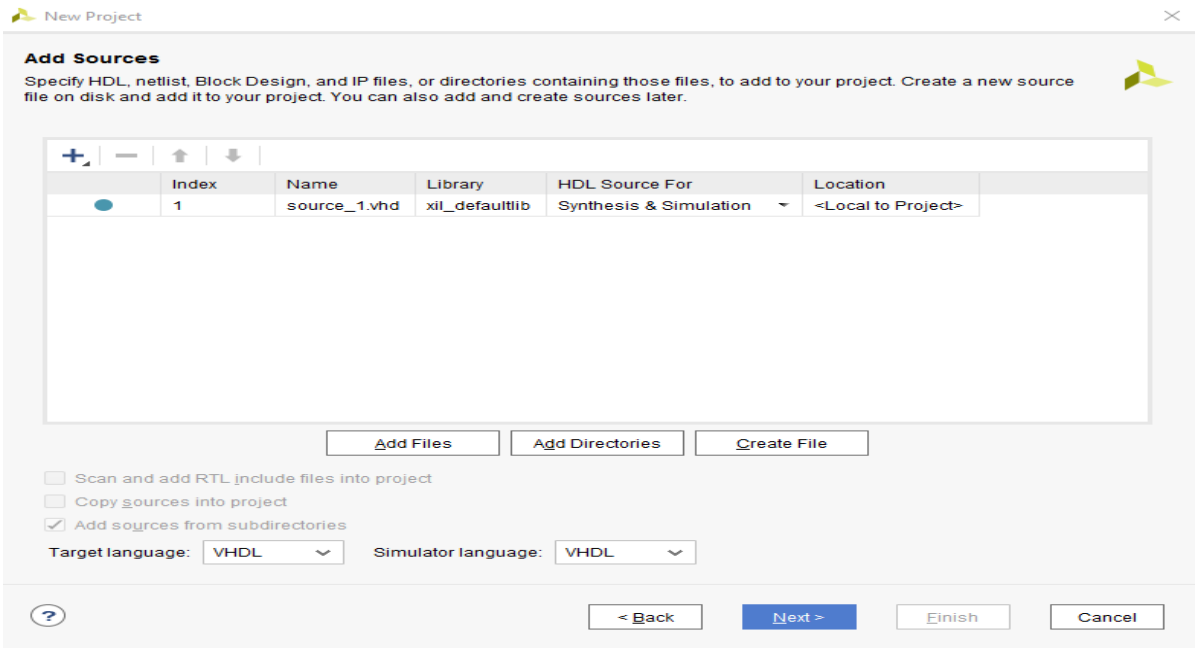


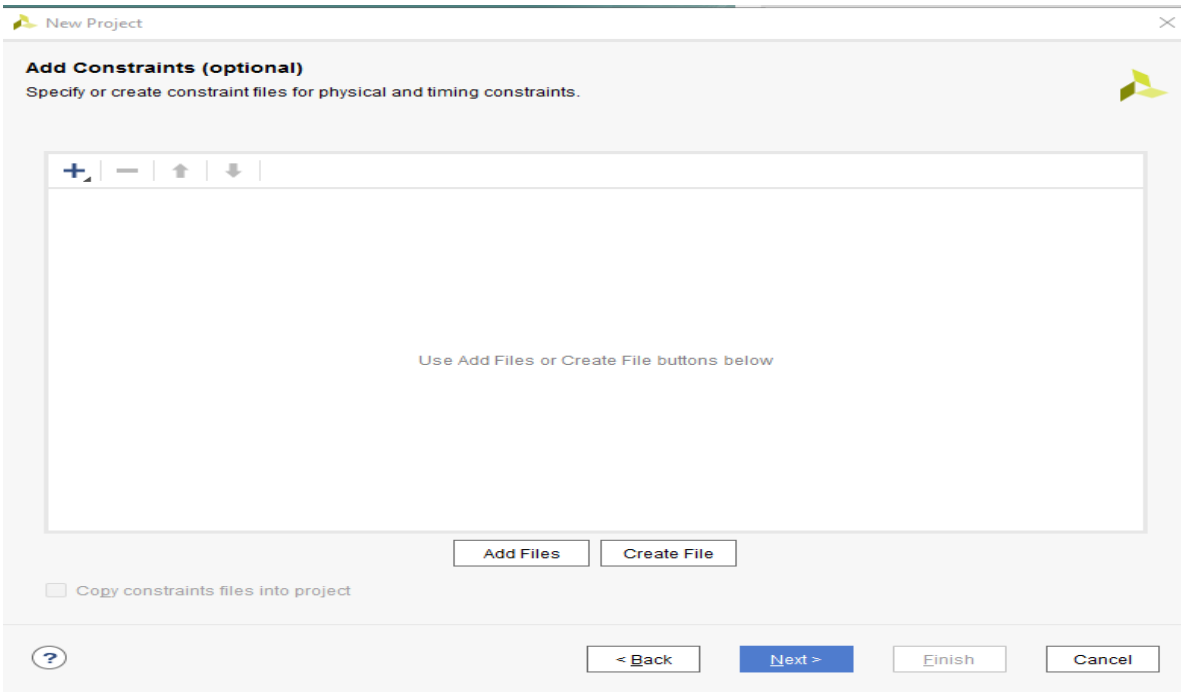
4. Choose “RTL Project” and check the “Do not specify sources at this time” as we will configure all the settings manually through the navigator from inside the project.

5. Select **New Source…** and the **New** window appears. In the New window, choose Schematic, type your file name (such as ***source_1***) in the File Name editor box, click on OK, and then click on the Next button.



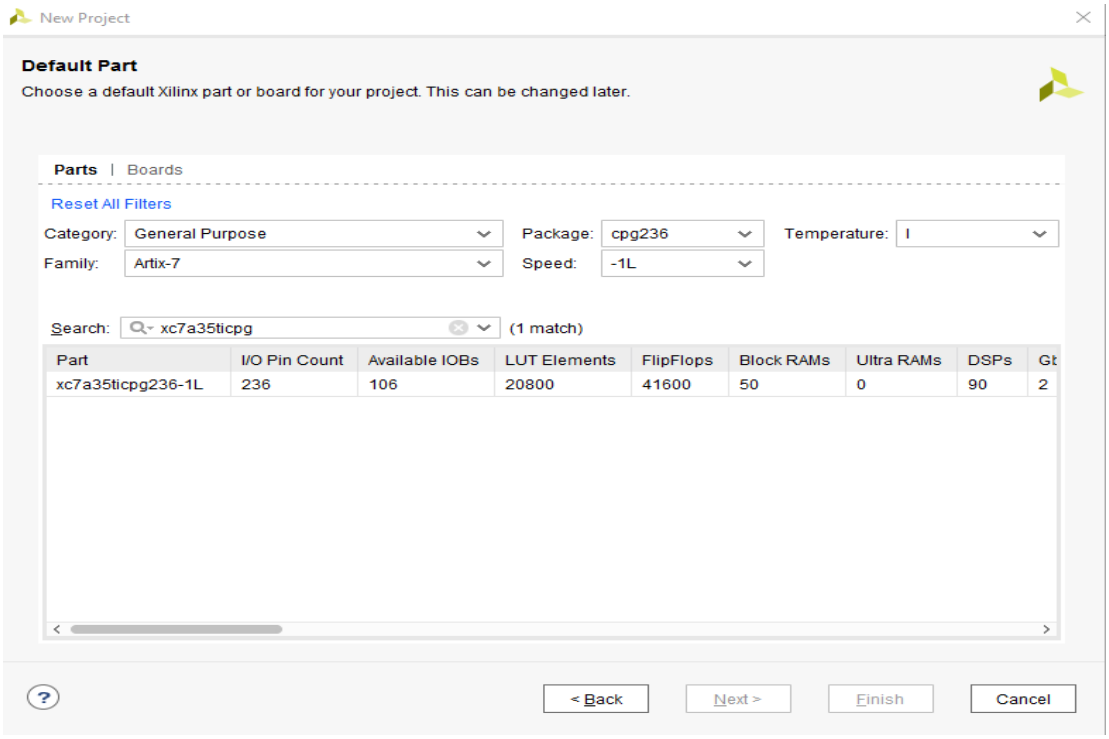


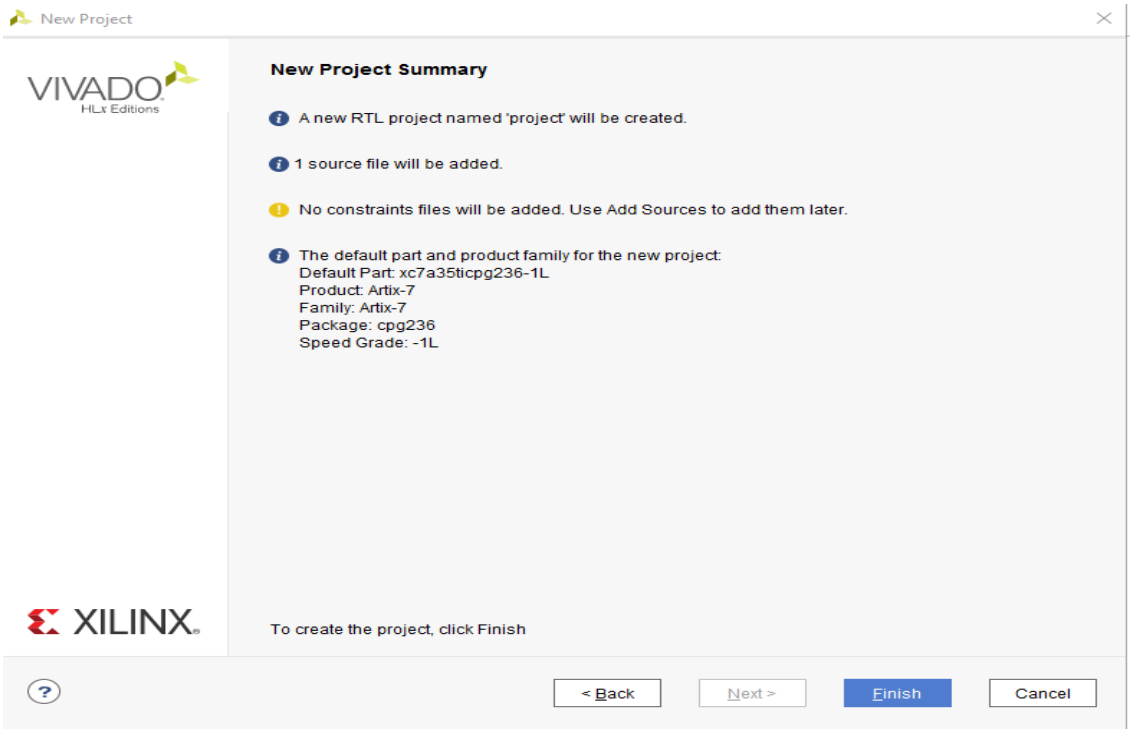




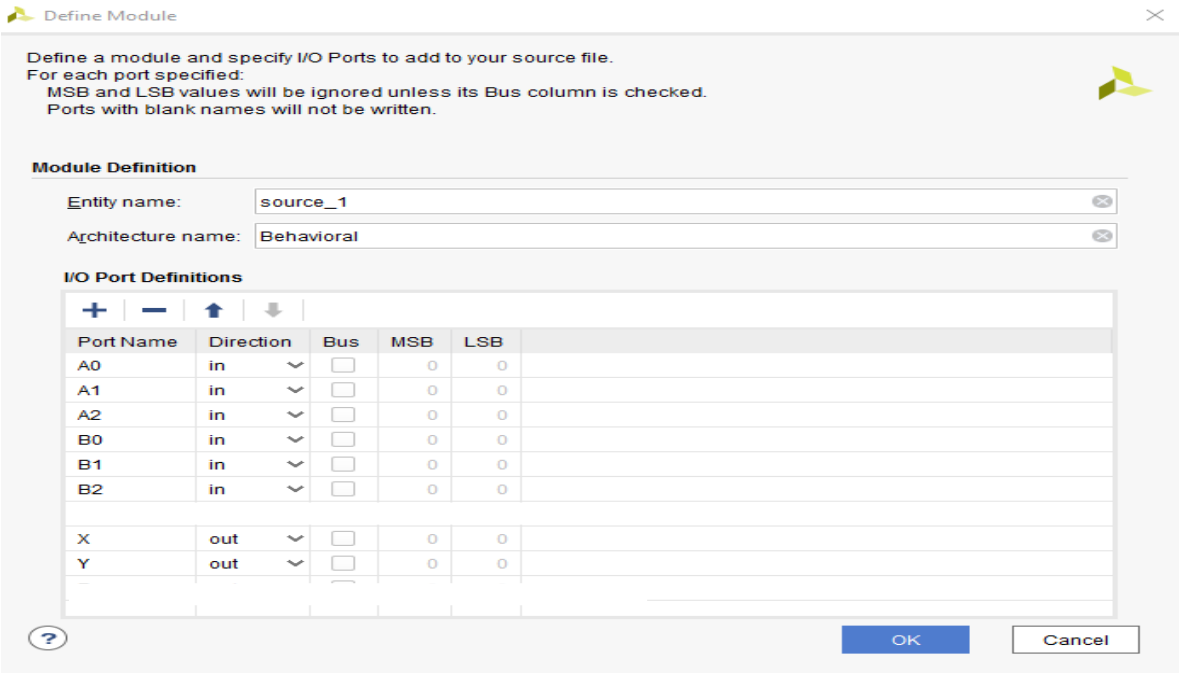
6. In the **Xilinx - Project Navigator** window, select the following
   - Category: "General Purpose"
   - Family: "Artix-7"
   - Package: "cpg236"
   - Speed: "-1"
   - Choose "xc7a35tcpg236-1" that corresponds to the board we are using.

Then Choose Finish.

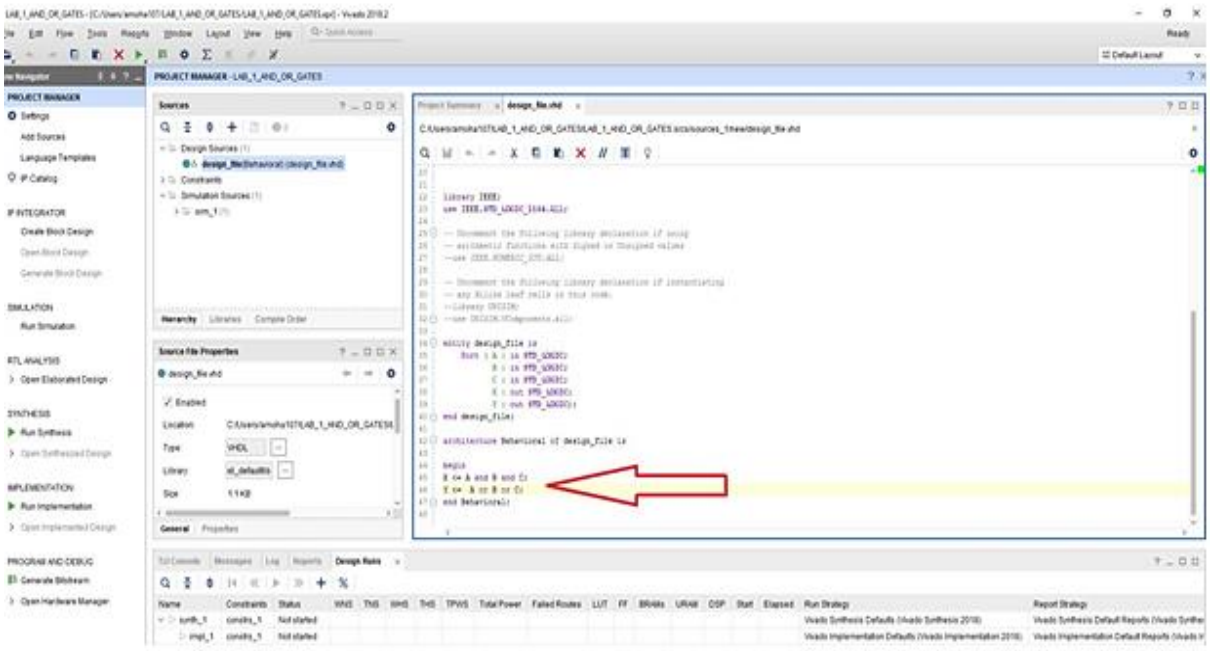




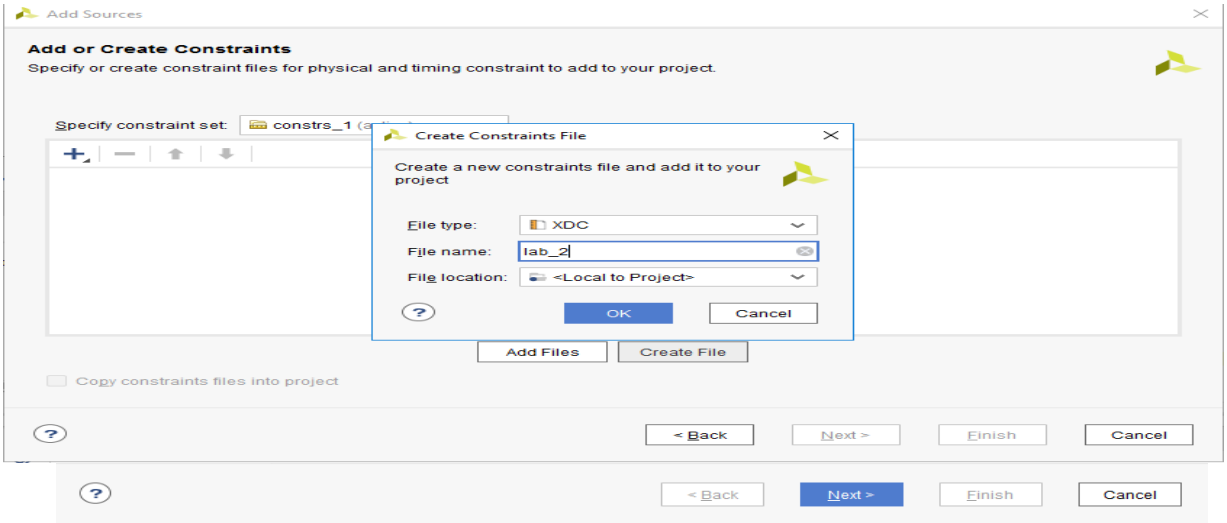
7. The Define Module Window that will appear, we will choose the input and output labels for the gates under investigation in this experiment. In this experiment, we are investigating a 3-input AND gate and 3-input OR. Then Under "Port Name", add "A0", "A1", "A2" as inputs for AND gate, add "B0", "B1" , "B2" as inputs for OR gate. Then add "X" & "Y" as outputs for the mentioned gates and select OK.



8. In the "source_1.vhd" created file, type the gates equivalent VHDL code for the AND & OR gates between the "begin" and "end Behavioral" as follows and then save the file.



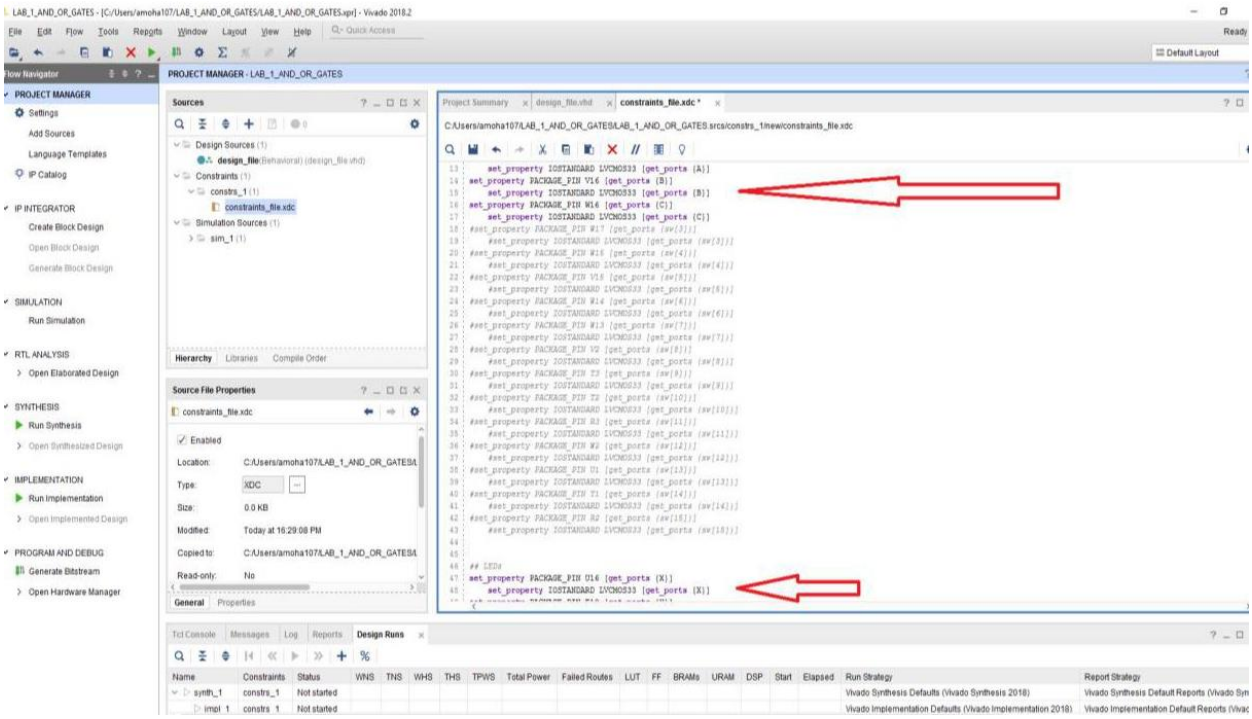
9. Next, we need to add To add a constraint file with the".xdc" extension, as following: Go to "Flow Navigator" and from "Project Manager" select "Add Sources" then "Add or create constraints". Next, choose "Create File" and enter the file name "lab_2" then "OK" followed by "Finish".



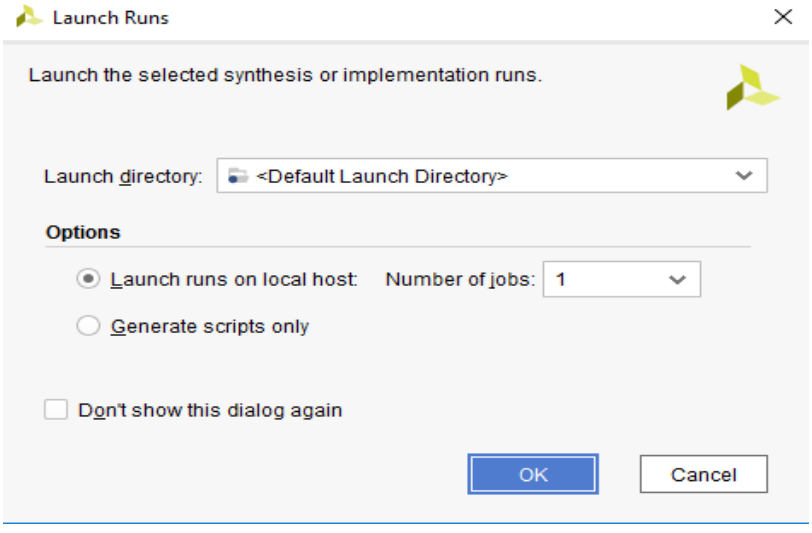
10. Then, we need to get a template xdc file that is going to be edited according to the different experiments. Google "basys 3 xdc file" and choose the "xilinix" link that appears (https://www.xilinx.com/support/documentation/university/Vivado-Teaching/HDL-Design/2015x/Basys3/Supporting%20Material/Basys3_Master.xdc).

Copy the whole file and paste it into the "lab_2.xdc" that you have just created in the last step. Then uncomment and edit the input Switches and the output LEDs as in the next step.

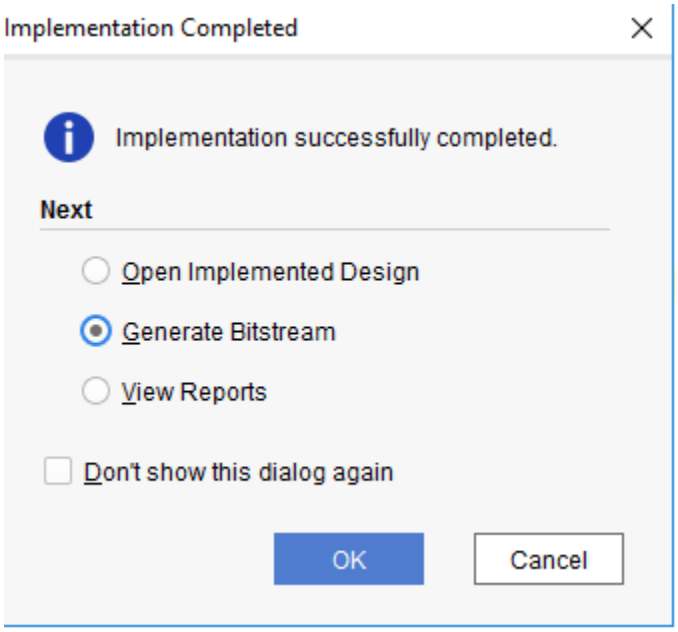
11. Uncomment (by deleting the # sign) sw[0], sw[1], sw[3],….. led[0], led[1],… lines. Note that each of them has two successive lines (Uncomment both of them). Do the following replacements: sw[0] ➔ A0, sw[1] ➔ A1,……, led[0] ➔ X, led[1] ➔ Y,…. , then Save the file



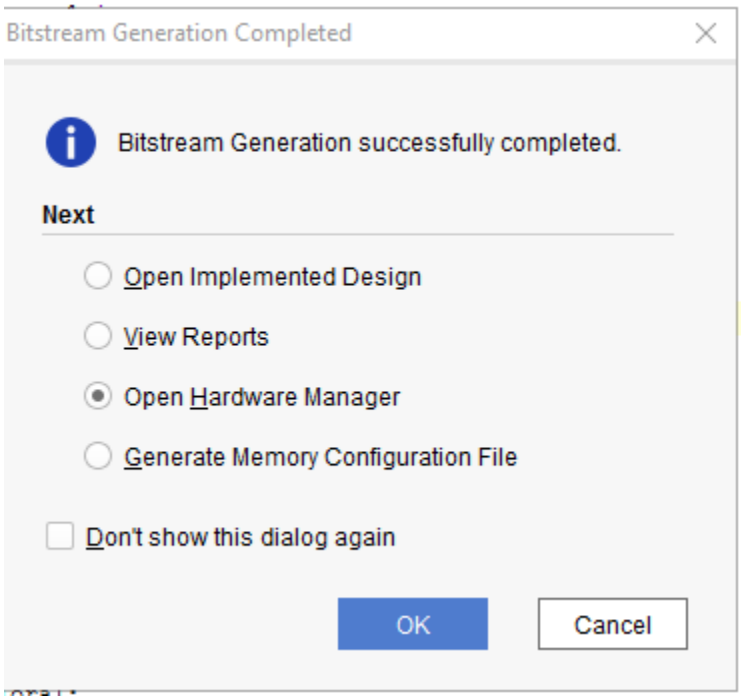
12. From the tool tab choose the play button ▶ and then "Run Implementation". Select "Number of jobs" =1 and then press OK.



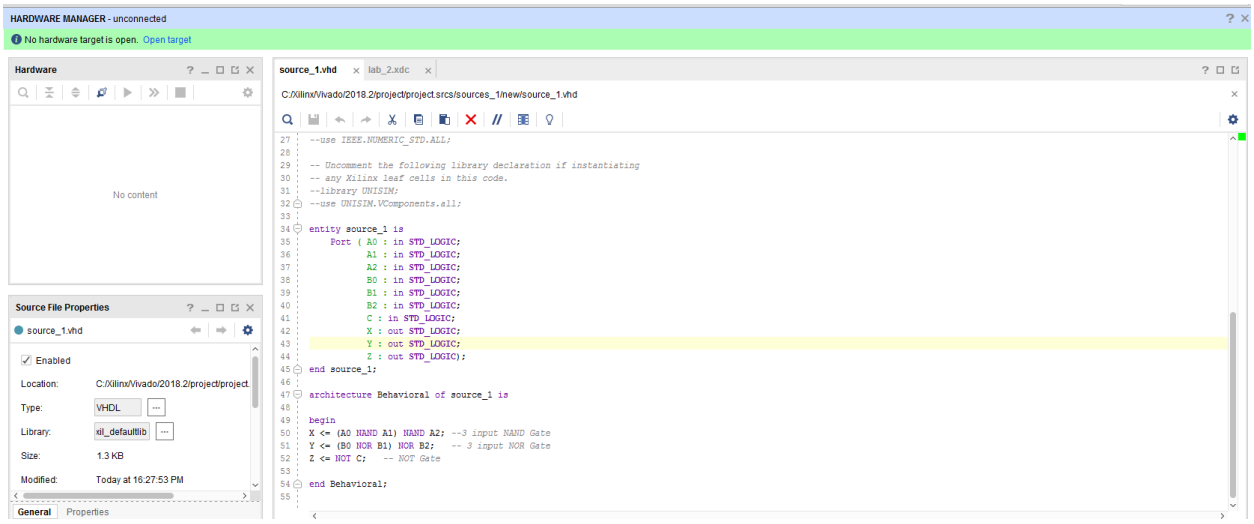
13. The implementation errors window will appear if any or the successfully completed window. From this window select “Generate Bitstream” and then OK. This will make the software generate “.bin” file to be used in programing the hardware BAYAS 3.



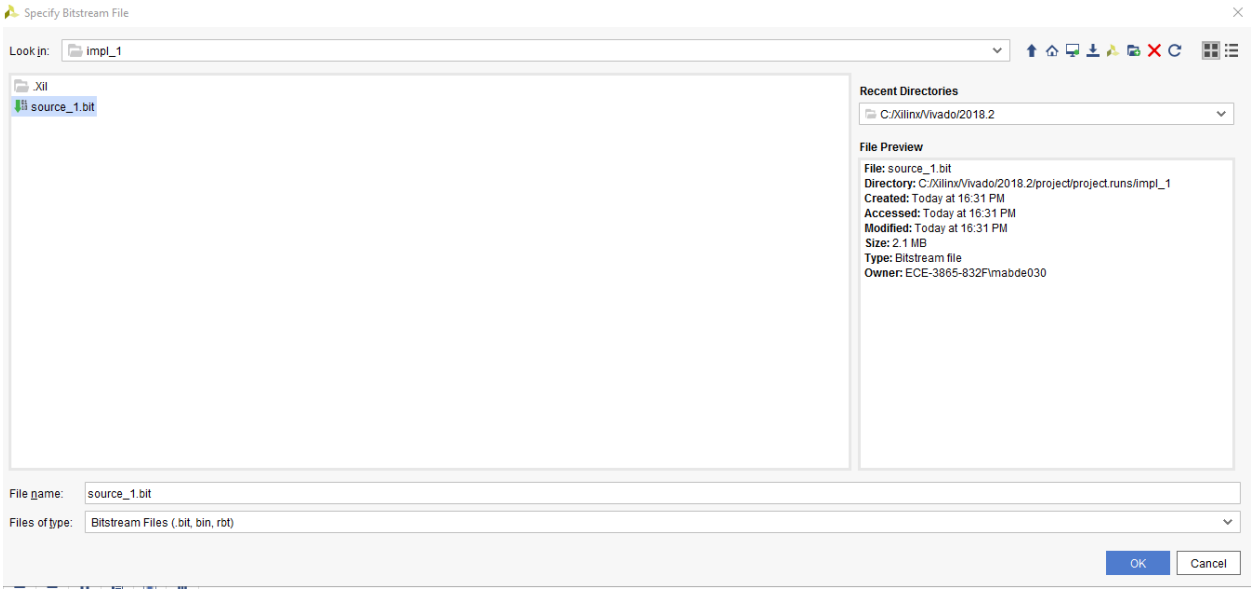
14. The next window will appear in which choose “Open Hardware Manger”, connect the Hardware Kit to the USB port and then press OK.



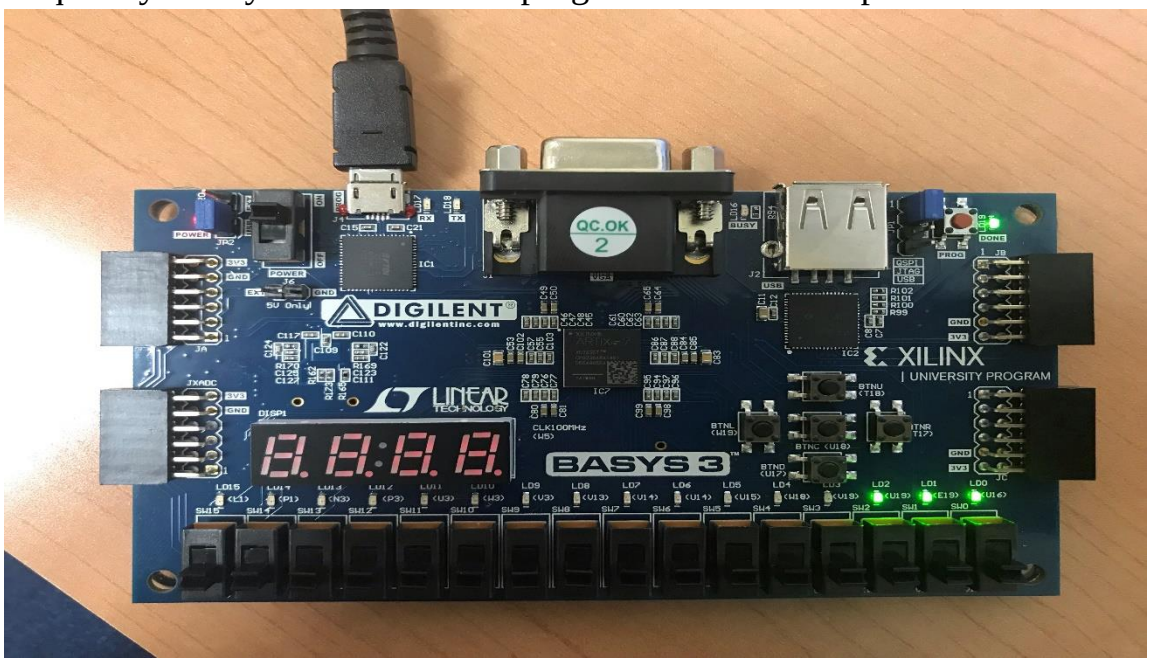
15. A green tab will appear in the top of the Vivado window, from which choose “open target” to program the hardware.



16. From the window appears, select the “.bin” file from the Project you create by browsing for the generated “.bit file” under the “.runs” folder and program the board then press OK.



17. Notice that the 7-segment on the hardware is counting up from 0 to 9 frequently until you download the program and it will stop.



18. Fill in the following truth tables for all the gates by observing the inputs/outputs on the programmed board.

A. AND Gate

Truth Table (1)

A0	A1	A2	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Symbol

Boolean Equation

B. OR Gate

Truth Table (2)

B0	B1	B2	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Symbol

Boolean Equation

19. Verify that the experimental results are consistent with the Discussion.

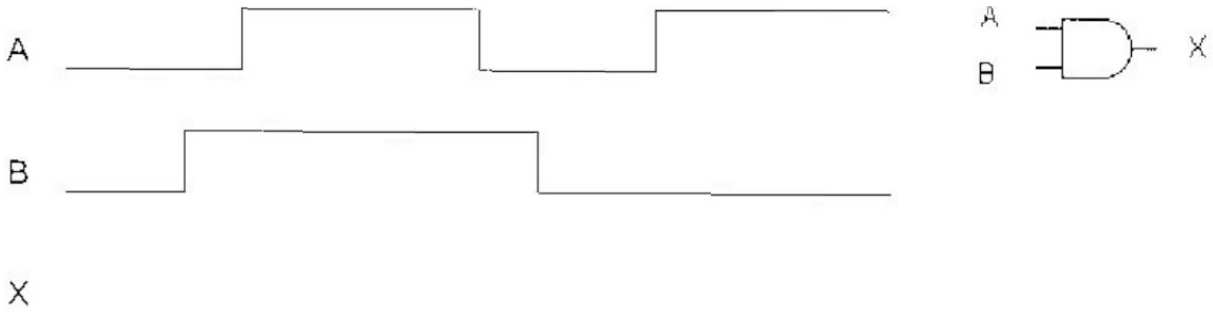
Checked by_____ Date _____

Questions:

1.) How many rows must a truth table have in order to describe a 4-input AND gate? Which input will make the output HIGH?

2.) Which output is the unique one in a 3-input OR gate? Does it agree with the statement in our Discussion section?

3.) Sketch the output waveform for the given NEXT



4.) In the Xilinx software symbol library, the maximum number of inputs for AND and OR gales is 9. What would you do if 10-input AND and OR gales are needed? Draw the schematic diagrams and show the connections.